

UG/3rd Sem/H/20 (CBCS)

2020

PHYSICS (Honours)

Paper : PHYH - DC-7T

[CBCS]

Full Marks : 25

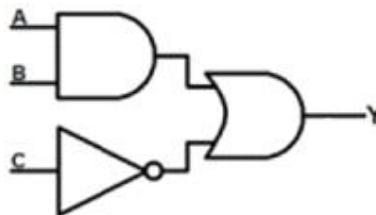
Time : Two Hours

*The figures in the margin indicate full marks.
Candidates are required to give their answers
in their own words as far as practicable.*

1. Answer any *five* questions :

2×5=10

- Show that $\overline{\overline{AB} + \overline{AB}} = AB + \overline{AB}$.
- Convert a hexadecimal number C5E2 to binary number. Convert a decimal number 2478 to hexadecimal number.
- Design a two-input XOR gate exclusively with the help of NAND gate.
- Obtain the Boolean expression for the output Y in the logic circuit of the figure given below

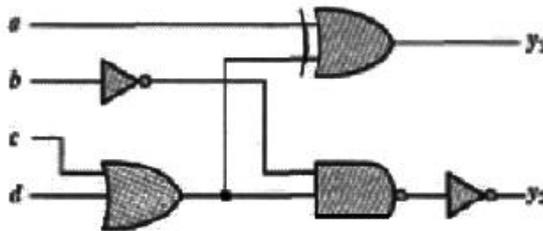


- Simplify the Boolean expression $Y = \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + A\overline{B}\overline{C}$ using a Karnaugh map.

- (f) Design a full adder using half adder.
- (g) Write the truth table of JK - flip-flop.
- (h) Write down the Boolean function corresponding to the following standard sum-of-product notation $f(A, B, C,) = \sum_m(3, 4, 6, 7)$.

2. Answer any *three* questions : 5×3=15

- (a) (i) Show that a positive logic NAND gate is a negative logic NOR gate and vice versa.
- (ii) Write a Boolean expression and construct the truth table describing the outputs of the circuits described by the logic diagram in the following figure. 2+3=5



- (b) What is encoder ? How encoder circuit can perform the decimal to BCD operation ? 1+4=5
- (c) What is a latch and how does it differ from a flip-flop ? Realize a D-flip-flop using NAND gates. 2+3=5
- (d) (i) Design a four bit shift registrar with parallel load using D flip-flop.
- (ii) Design a four-bit binary synchronous up counter with D flip-flop. 3+2=5
- (e) Design an astable multivibrator using a 555-timer. 5